

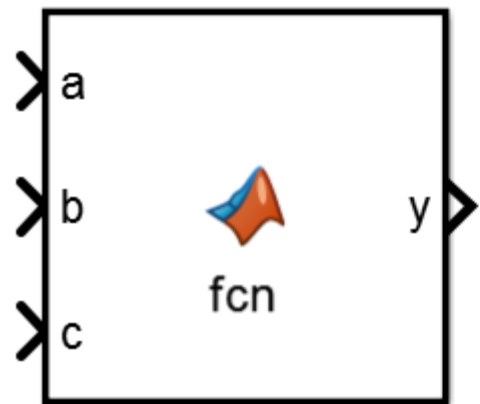
# Simulink for Signal Processing Algorithm Development

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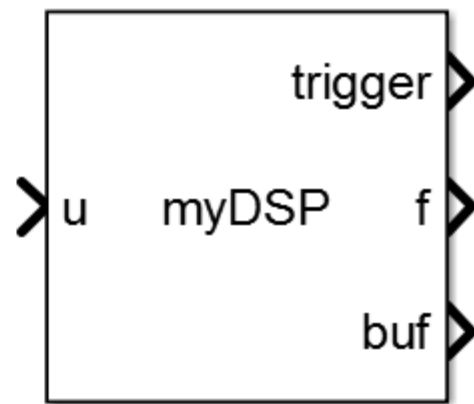
*Use **MATLAB** for **algorithm design***

*Use **Simulink** for **system design***

# 1. Simulink speaks MATLAB



MATLAB Function



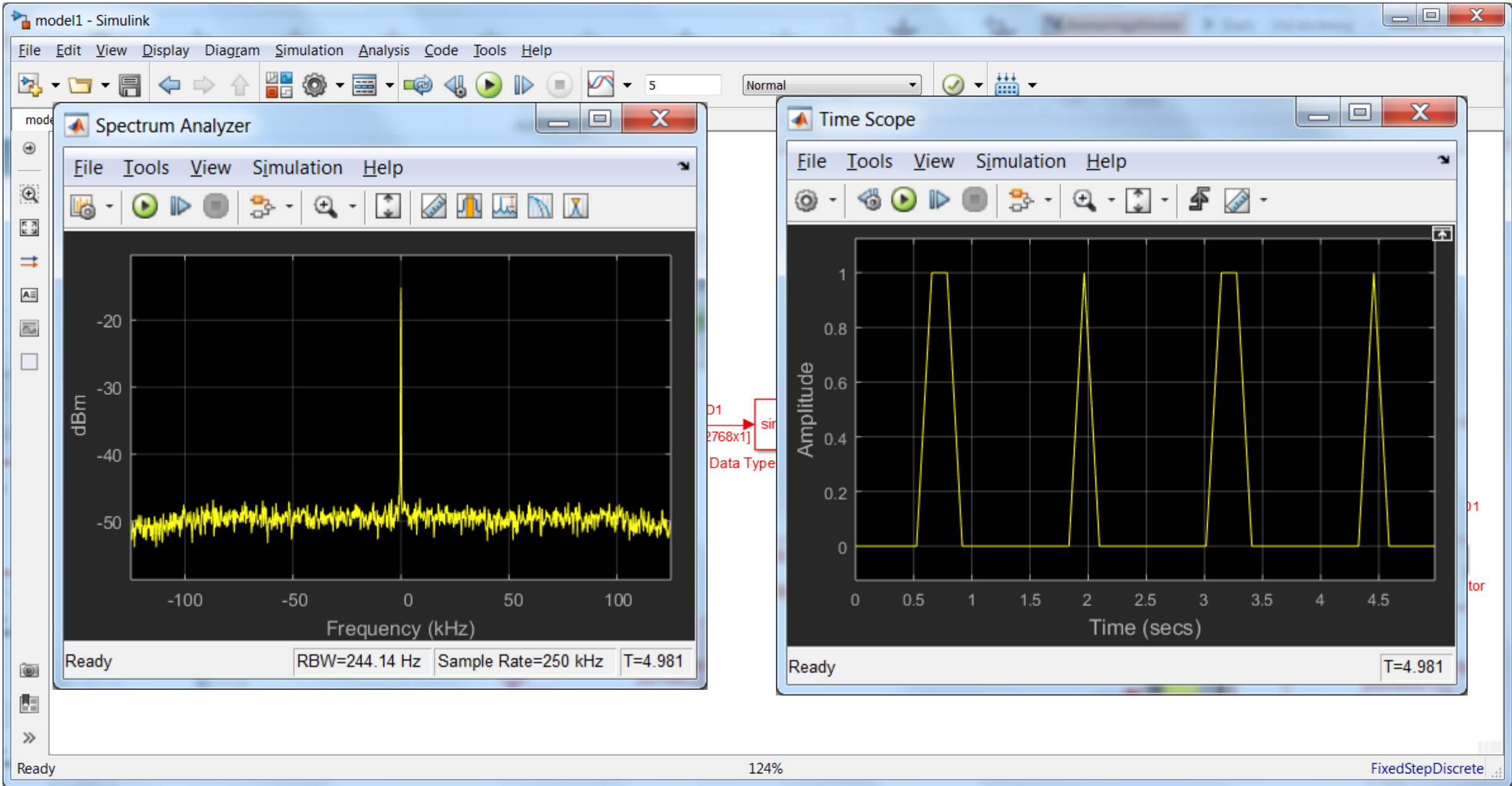
MATLAB System



# (... and MATLAB speaks Simulink)

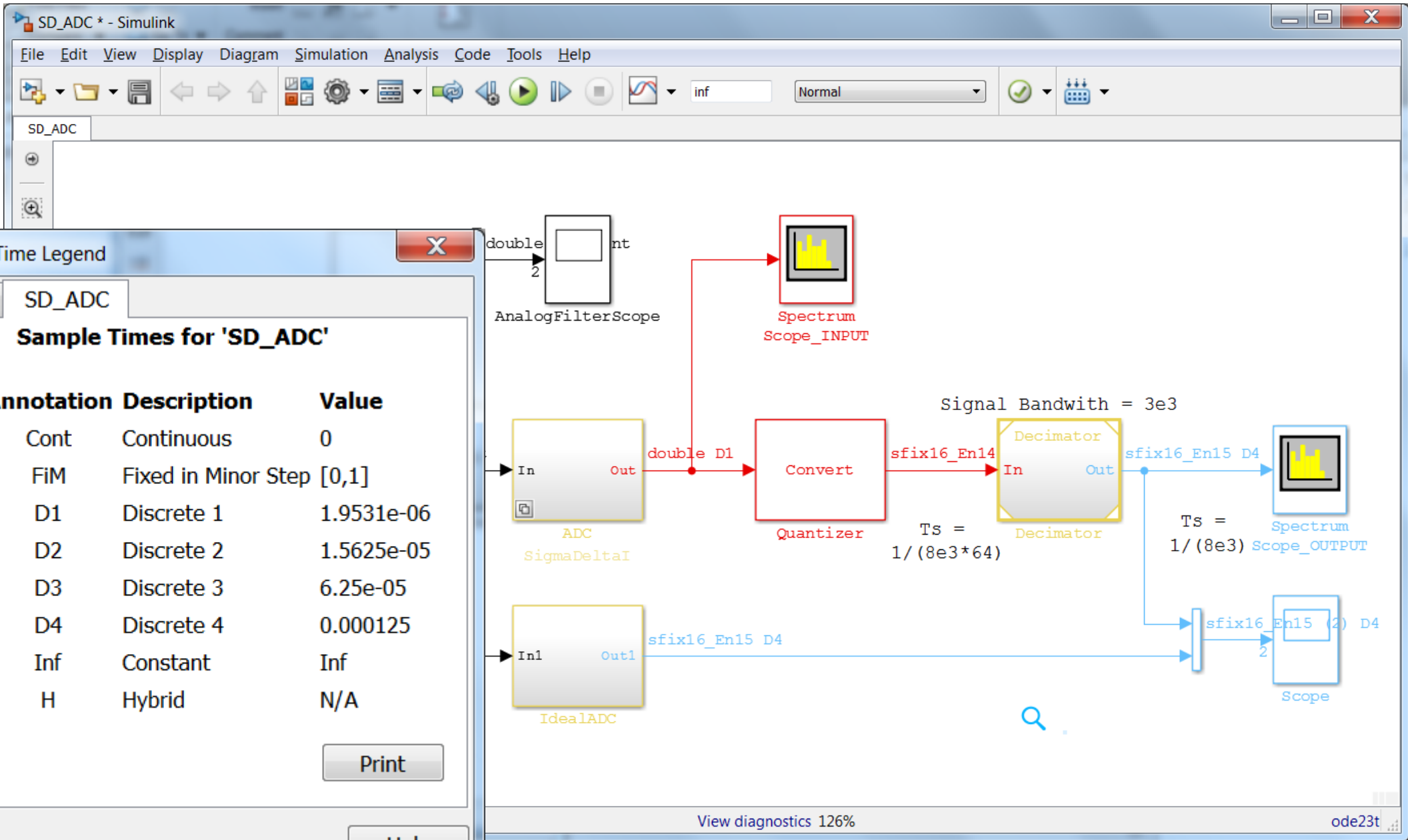
```
parfor idx=1:iterations
    simout(idx) = sim(model, 'SimulationMode', 'normal');
end
```

- 1. Simulink speaks MATLAB**
- 2. Simulink knows what time it is**



- 1. Simulink speaks MATLAB**
- 2. Simulink knows what time it is**
- 3. Simulink handles multirate systems**





Sample Time Legend

model1 SD\_ADC

**Sample Times for 'SD\_ADC'**

Color Annotation	Description	Value	
Black	Cont	Continuous	0
Grey	FiM	Fixed in Minor Step	[0,1]
Red	D1	Discrete 1	1.9531e-06
Green	D2	Discrete 2	1.5625e-05
Blue	D3	Discrete 3	6.25e-05
Light Blue	D4	Discrete 4	0.000125
Pink	Inf	Constant	Inf
Yellow	H	Hybrid	N/A

Print

Help

- 1. Simulink speaks MATLAB**
- 2. Simulink knows what time it is**
- 3. Simulink handles multirate systems**
- 4. Simulink has continuous time**

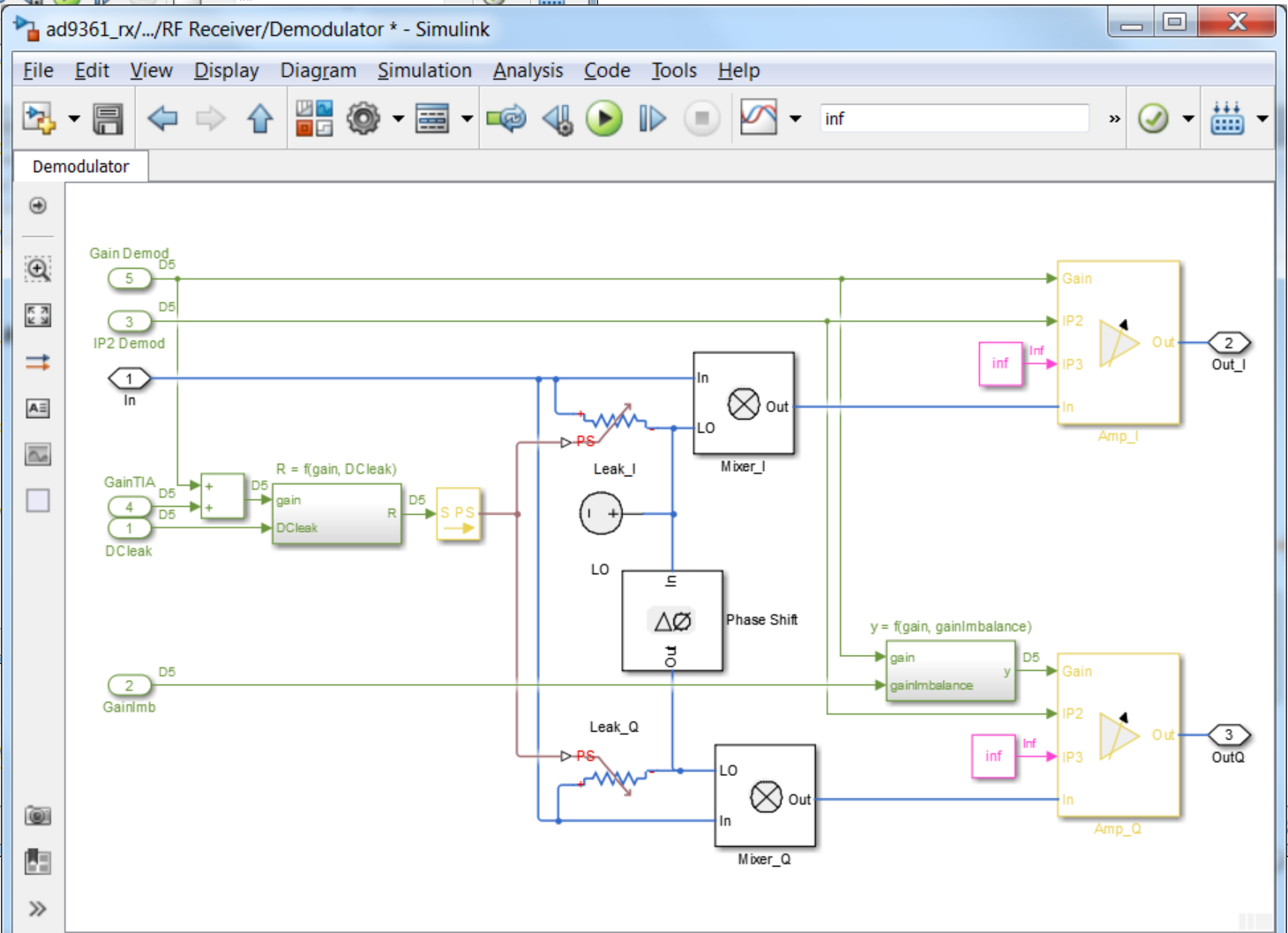
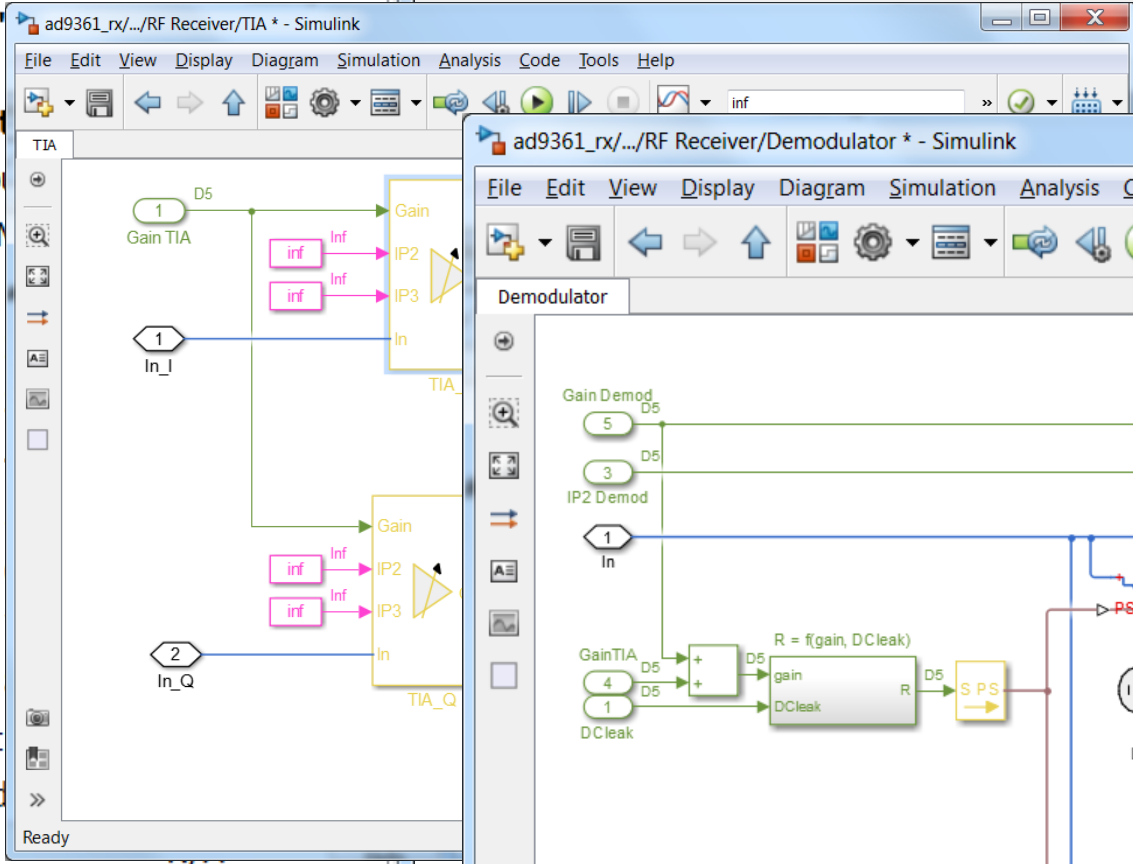
### Sample Time Legend

ad9361\_rx

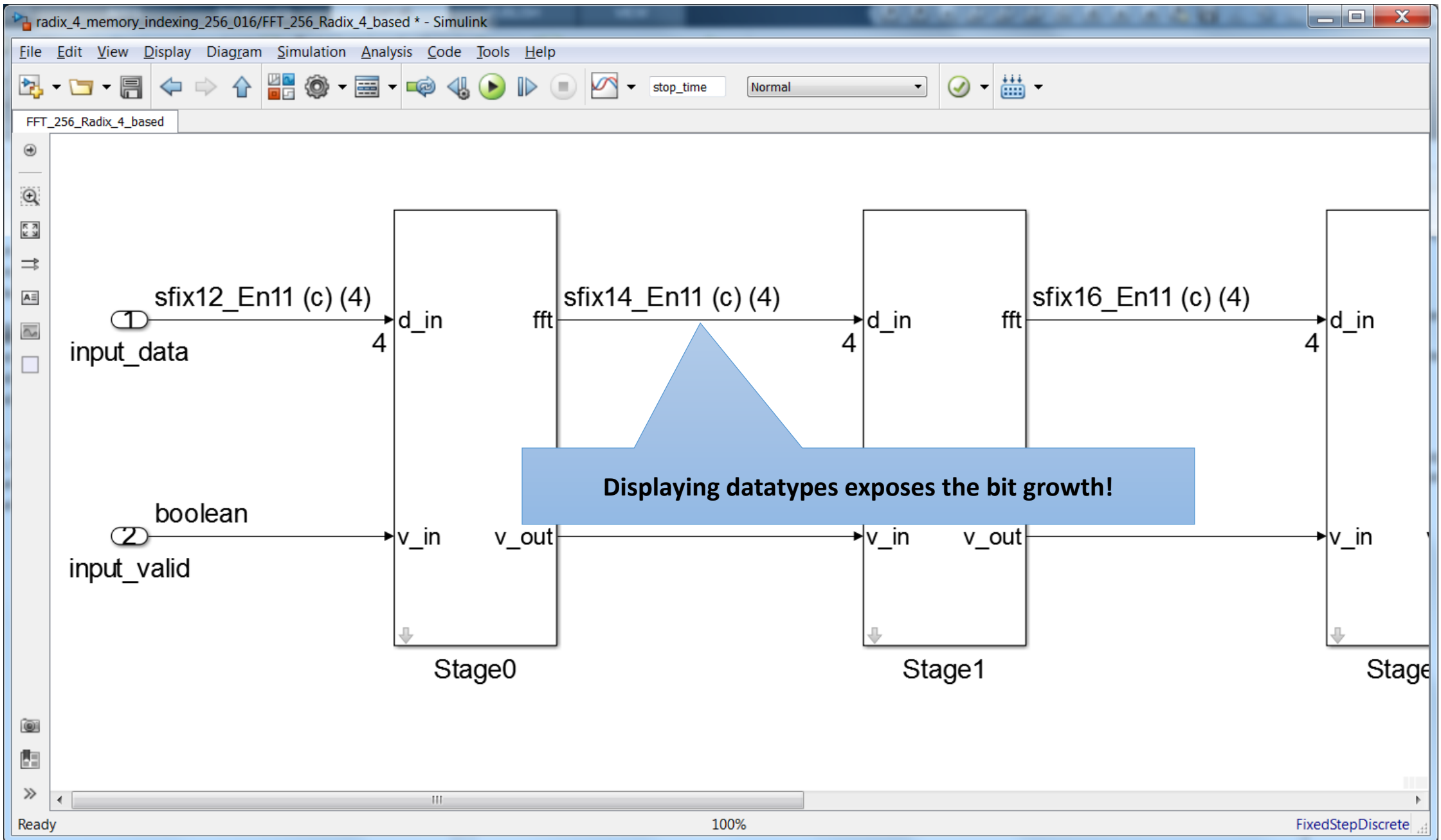
#### Sample Times for

Color	Annotation	Description
Black	Cont	Continuous
Grey	FIM	Fixed in M
Red	D1	Discrete
Green	D2	Discrete
Blue	D3	Discrete
Light Blue	D4	Discrete
Olive Green	D5	Discrete
Orange	D6	Discrete
Light Orange	D7	Discrete
Dark Orange	D8	Discrete
Pink	Inf	Constant
Cyan	T1	Triggered
Yellow	H	Hybrid

Print Help



- 1. Simulink speaks MATLAB**
- 2. Simulink knows what time it is**
- 3. Simulink handles multirate systems**
- 4. Simulink has continuous time**
- 5. Simulink shows datatypes**



- 1. Simulink speaks MATLAB**
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- 3. Simulink handles multirate systems**
- 4. Simulink has continuous time**
- 5. Simulink shows datatypes**
- 6. Simulink maps well to HW/SW arch.**

gm\_my\_equalizer\_sim\_optimization/.../filter\_subsystem/filter\_bank\_left

File Edit View Display Diagram Simulation Analysis Code Tools Help

Model Browser

- gm\_my\_equalizer\_sim\_optimization
  - Demux
  - EqualizerAlgorithm
    - EQ\_Parameters
    - filter\_subsystem
      - filter\_bank\_left
      - filter\_bank\_right
    - LCD2Display

filter\_bank\_left

1 input

-C- s(1) coeff

-C- a(2)(1) coeff

-C- a(3)(1) coeff

2 parameters

Filter

Output

3 gain

z<sup>-2</sup> rd\_1

gain11

cd\_0

data\_out

Ready 136% FixedStepDiscrete

HDL Code generation report

Contents

- Summary
- Clock Summary
- Resource Utilization Report
- Optimization Report
  - Distributed Pipelining
  - Streaming and Sharing
  - Traceability Report
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  - Next
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  - Equalizer\_Subsystem\_pka.vhd
  - filter.vhd
  - Filter1.vhd
  - Filter2.vhd
  - Filter3.vhd
  - Filter4.vhd
  - Filter5.vhd
  - Filter6.vhd
  - Filter7.vhd
  - Filter8.vhd
  - Filter9.vhd
  - filter\_bank\_left.vhd
  - effect\_selection.vhd
  - parameter\_lookup.vhd
  - Equalizer\_Subsystem.vhd (2)

```
278     IF reset = '1' THEN
279         Input_Register1_out1 <= to_signed(0, 16);
280     ELSIF enb = '1' THEN
281         Input_Register1_out1 <= right_in_signed;
282     END IF;
283 END IF;
284 END PROCESS Input_Register1_process;
285
286
287 filter_bank_right_out1_signed <= signed(filter_bank_right_out1);
288
289 -- <S1>/Output_Register1
290 --
291 --
292 -- Block requirements for <S1>/Output_Register1
293 -- 1. Design must be synchronous
294 Output_Register1_process : PROCESS (clk)
295 BEGIN
296     IF clk'EVENT AND clk = '1' THEN
297         IF reset = '1' THEN
298             Output_Register1_out1 <= to_signed(0, 16);
299         ELSIF enb = '1' THEN
300             Output_Register1_out1 <= filter_bank_right_out1_signed;
301         END IF;
302     END IF;
303 END PROCESS Output_Register1_process;
304
305
306 right_out <= std_logic_vector(Output_Register1_out1);
307
308 ce_out <= clk_enable;
309
310 END rtl;
311
312
```