MATLAB EXPO

# Intel® Agilex™ 7 FPGA-in-the-Loop Simulation

## Enabling DSP Emulation for Space-BACN

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# DARPA Space-BACN Program

Space-Based Adaptive Communications Node (**Space-BACN**) program aims to create to create **a reconfigurable intersatellite optical communications terminal** that is low size, weight, power, and cost (SWaP-C), and easy to integrate.

It allows seamless **communication between heterogeneous constellations** that operate on different optical intersatellite link (OISL) specifications, and which otherwise would not be able to communicate.

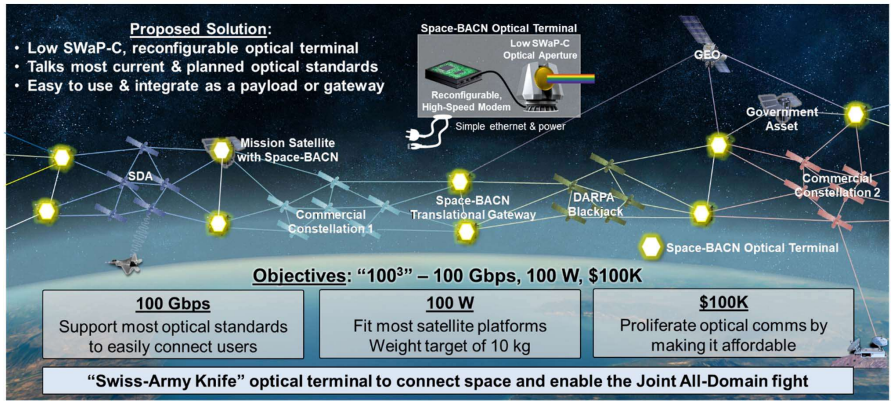
The program objectives are summarized as "100 Cubed":

- 100 Gbps to support most optical standards.
- 100W or less to minimize power consumption.
- Under $100K to make it affordable.

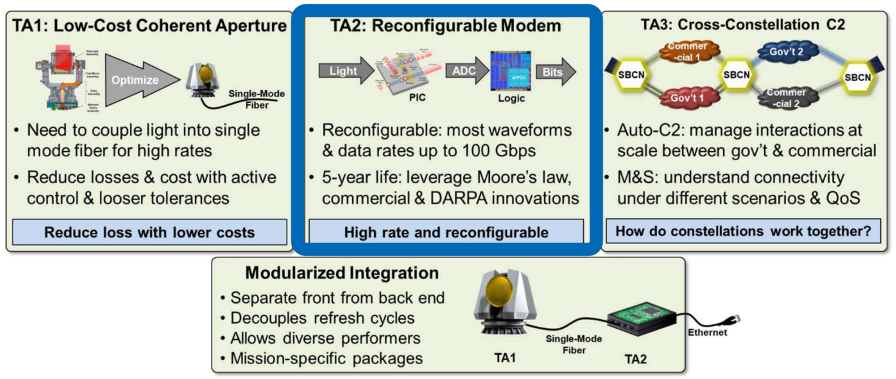
Space-BACN will focus on three key technical areas:

- A low-cost, optical aperture capable of coupling into single mode fiber Lower-risk design integration (TA1).
- A reconfigurable modem that can support multiple optical waveforms up to 100 Gbps (TA2).
- A novel cross-constellation command and control approach to automate interactions between government and commercial satellites (TA3).

https://www.darpa.mil/work-with-us/space-based-adaptive-communications-node




Space-BACN program overview




Space-BACN program components

# TA2 Requirements & DSP Implementation Considerations

Digital Signal Processing (DSP) Emulation Considerations:

- Modulation/Demodulation Formats
  - OOK, PPM, DPSK, BPSK, QPSK, and DP-QPSK
- Datarates
  - Up to 10Gbps OOK & Up to 100Gbps PSK
- Timing Recovery Loops
  - Clock Data Recovery (CDR)
  - Doppler + CDR
- FEC coding
  - DVB-S2 (LDPC+BCH), SDA (LDPC), OFEC (Turbo), CCSDS (RS, LDPC), G709 (RS)
- Post-FEC BER
  - ≤1E-15

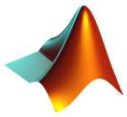
| TA2 Metric | Phase 1 | Phase 2 |
|---|---|---|
| Supported modulation formats | Reconfigurable design for OOK, PPM, DPSK, BPSK, QPSK, and DP-QPSK | EDU reconfigurable for OOK, PPM, DPSK, BPSK, QPSK, and DP-QPSK |
| Baud rate | Programmable 1-33 GBaud | Programmable 1-33 GBaud |
| Supported data rates | Up to 10 Gbps OOK<br>up to 100 Gbps PSK | Up to 10 Gbps OOK<br>up to 100 Gbps PSK |
| Transmitter | | |
| Tunable/selectable wavelength range | 1,530 nm – 1,565 nm | 1,530 nm – 1,565 nm |
| Laser RIN | -140 dB/Hz peak<br>-145 dB/Hz average | -140 dB/Hz peak<br>-145 dB/Hz average |
| Laser spectral linewidth | 500 kHz | 500 kHz |
| Optical output measured in SMF | 0 dBm per polarization | 0 dBm per polarization |
| TX OSNR | >30 dB/0.1 nm | >30 dB/0.1 nm |
| TX output polarization | PM-SMF | PM-SMF |
| Receiver | | |
| Sensitivity at 100G | - 18 dBm | - 18 dBm |
| Post-FEC BER | ≤1E-15 | ≤1E-15 |
| Optical input | SMF | SMF |
| FEC coding supported (code rates ≥1/2) | DVB-S2 (LDPC+BCH), SDA (LDPC), OFEC (Turbo), CCSDS (RS, LDPC), G709 (RS) | Phase 1 + programmable to other variants |
| Doppler | Up to ±50 ppm | Up to ±50 ppm |

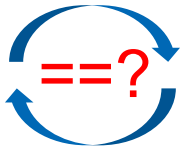
Space-BACN program TA2 metrics

https://sam.gov/opp/e704657b448649a4a5ff7debeb39540a/view
Space_BACN_Appendix_amended_20210927.pdf

# DSP Simulation Challenges and Solutions

Does the design implemented in HDL match the specification?

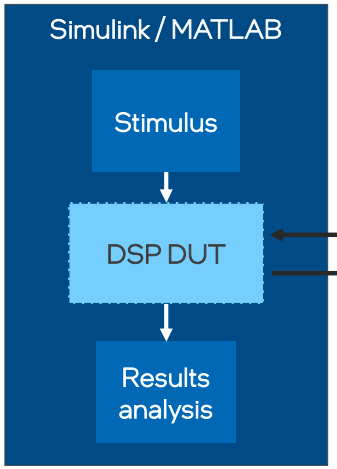





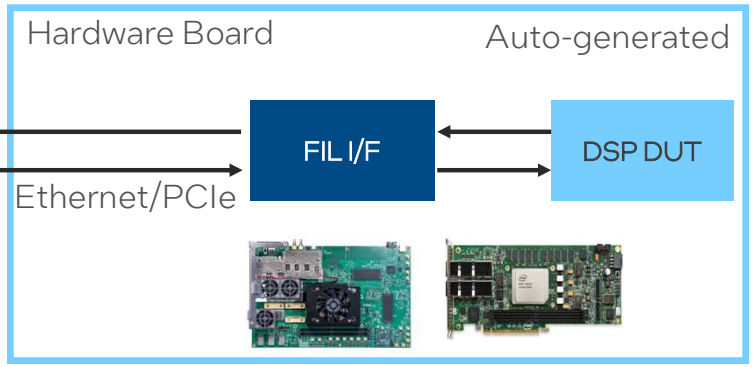

RTL

Algorithm Design as Specification

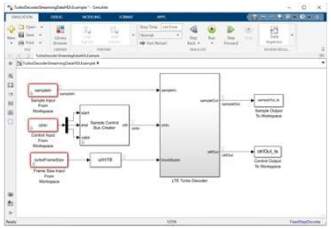
Implemented Hardware Design



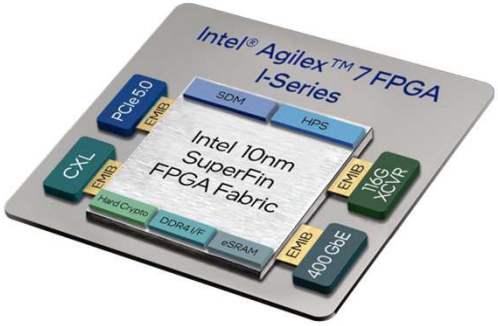

MATLAB/Simulink as Test Bench for Hardware IP FPGA-in-the-Loop (FIL)




Software simulation is SLOW!



Processing 16B+ samples of LTE Turbo Decoder test stimulus can take 21.5 days

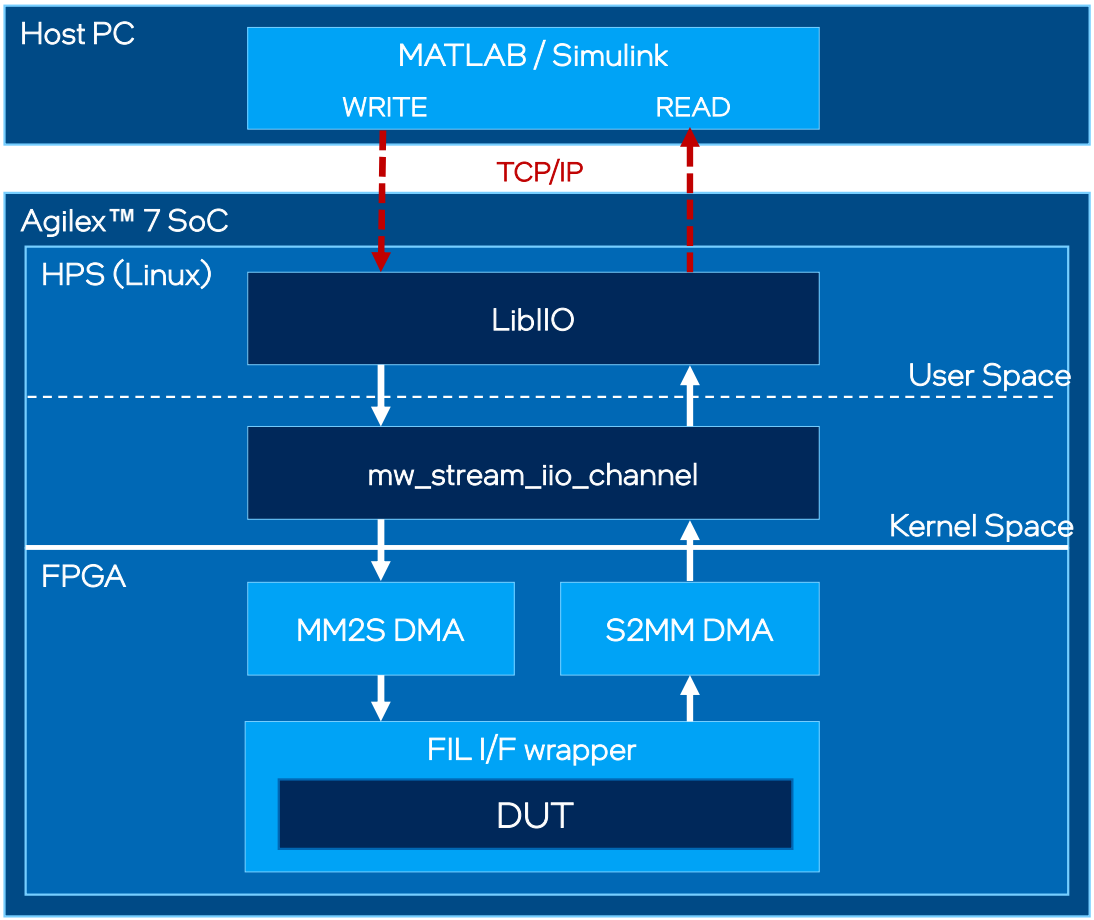


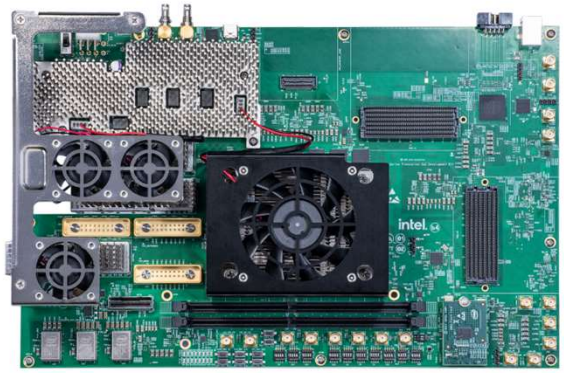

https://www.intel.com/content/www/us/en/products/details/fpga/agilex/7/i-series.html

Relevant Key Features:

- PCI Express (PCIe) 5.0 Support
- Hard Processor System (HPS)
  - Quad-core Arm Cortex-A53
- AGI 027
  - 2700 KLE
  - DDR4

# Ethernet FIL Architecture for Agilex



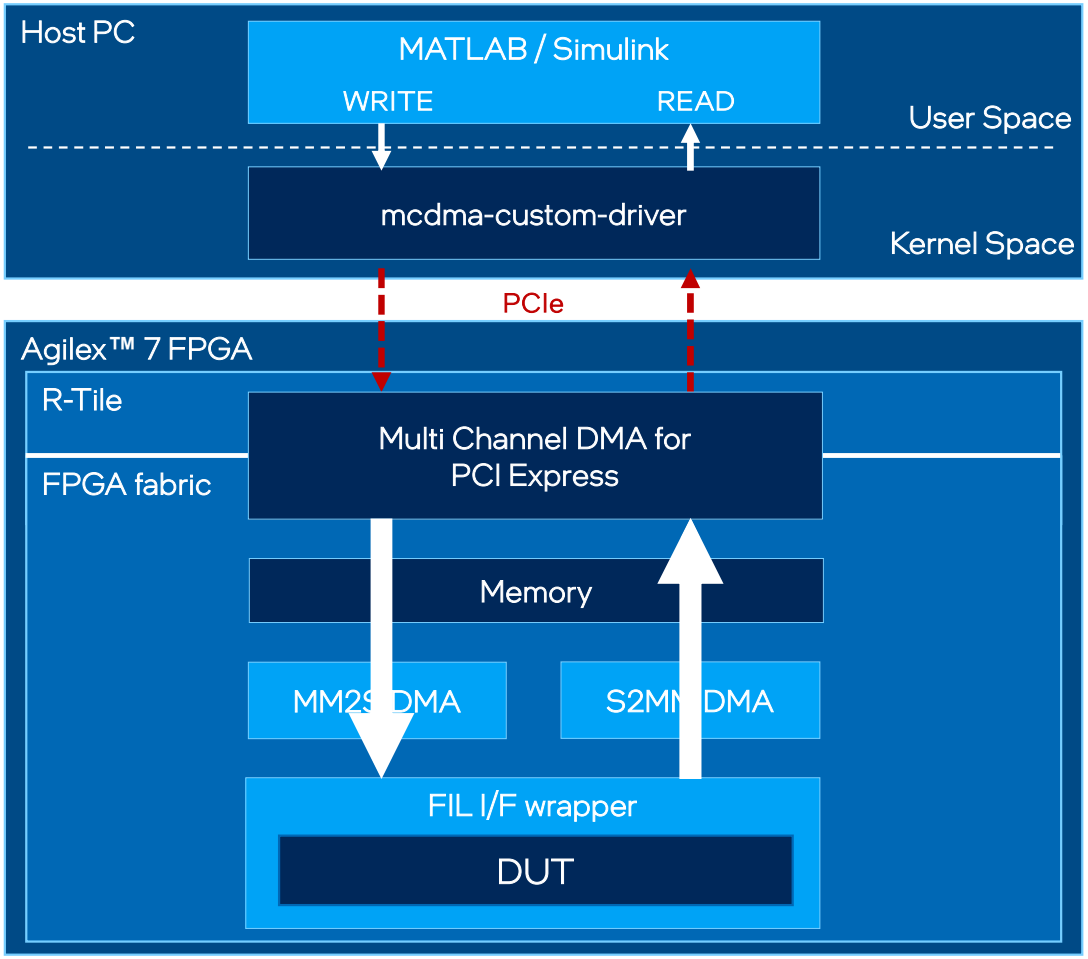



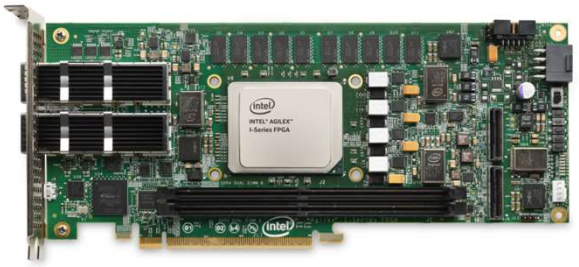
Intel® Agilex™ 7 FPGA I-Series Transceiver-SoC Development Kit (4x F-Tile) DK-SI-AGI027FB

https://www.rocketboards.org/foswiki/Documentation/AgilexSoCGSRDSIAGI027

https://github.com/mathworks/altera-linux/tree/mw-agilex-soc-5.15/drivers/misc/mathworks

# PCI-Express FIL Architecture for Agilex (On-going)



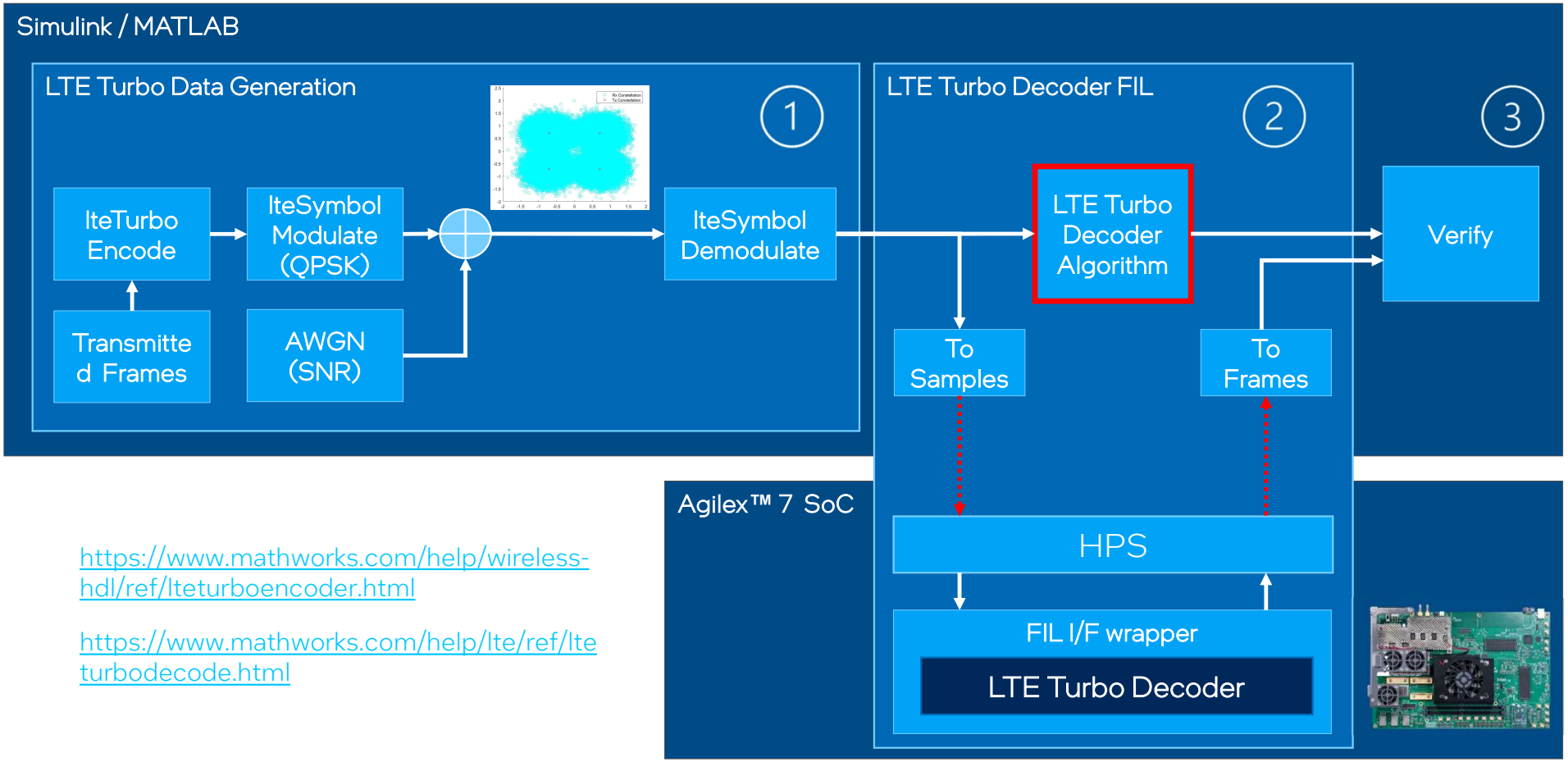



Intel® Agilex™ 7 FPGA I-Series Development Kit (2x R-Tile and 1x F-Tile) DK-DEV-AGI027R1BES

https://www.intel.com/content/www/us/en/docs/programmable/683821/22-4/

https://www.intel.com/content/www/us/en/docs/programmable/683517/22-4/

# FIL Simulation Demo - LTE Turbo Decoder

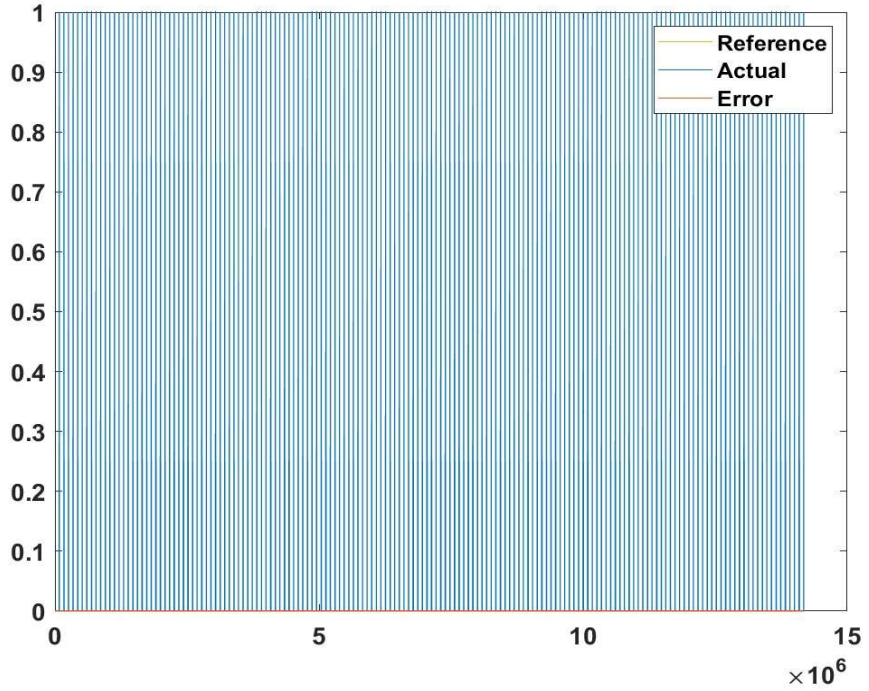



https://www.mathworks.com/help/wireless-hdl/ref/lteturboencoder.html

https://www.mathworks.com/help/lte/ref/lteturbodecode.html

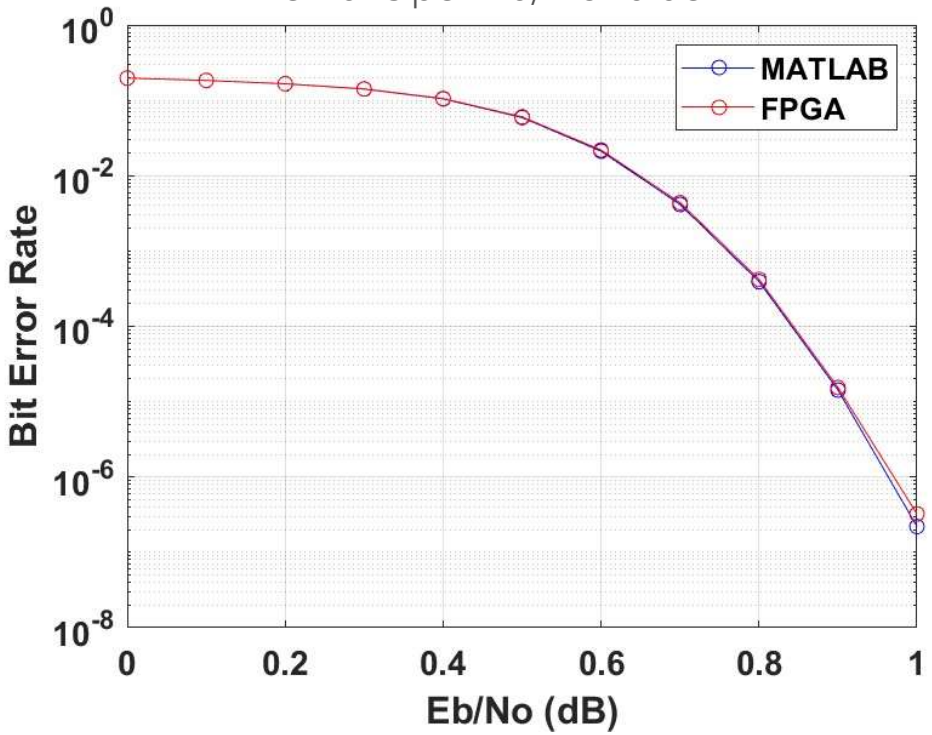
# FIL Simulation Demo - Results

Decoded bits - Sim vs. FIL (1e6 bits, Eb/No = 0.5)




- Bit and cycle accuracy between the hardware module and the source Simulink model used to generate the RTL code

1e9 bits per Eb/No value




- Simulation: 518 hours (21.5 days)
- FIL cycle accurate: 48 hours (2 days)
- FIL free running: 23 minutes

# Notices & Disclaimers

This research was, in part, funded by the U.S. Government under the DARPA Space-BACN program. The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressed or implied, of the U.S. Government.

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