



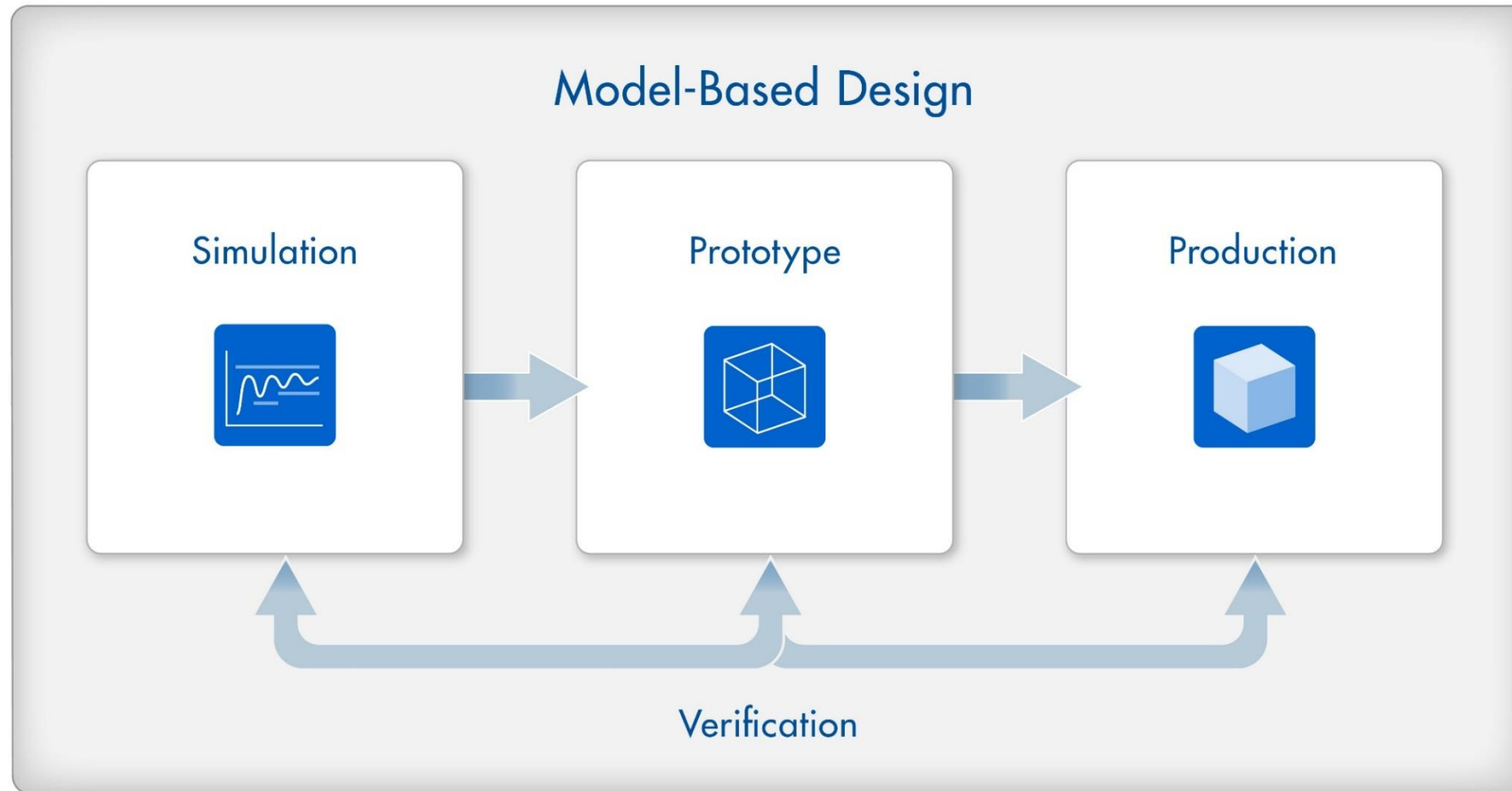
# Algorithm Development Using Model-Based Design

Eric Cigan  
MathWorks



# Model-Based Design

A single shared development environment

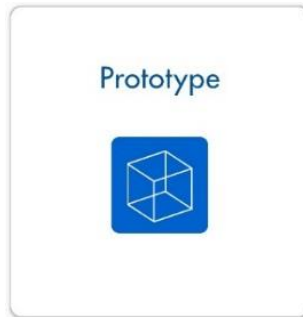


# Model-Based Design

A single shared development environment



**Verify operation before committing to hardware**

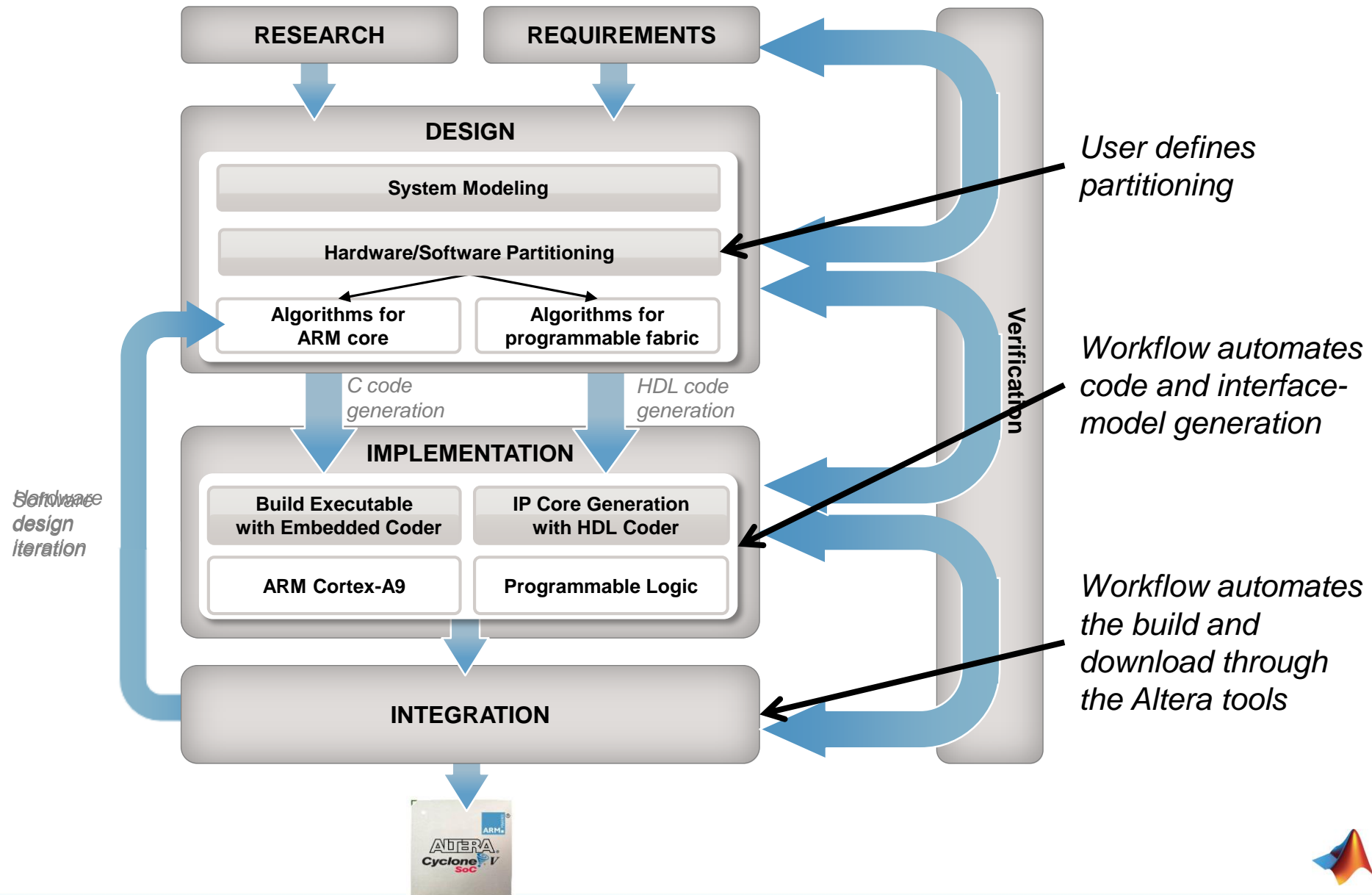


**Validate performance on chip**

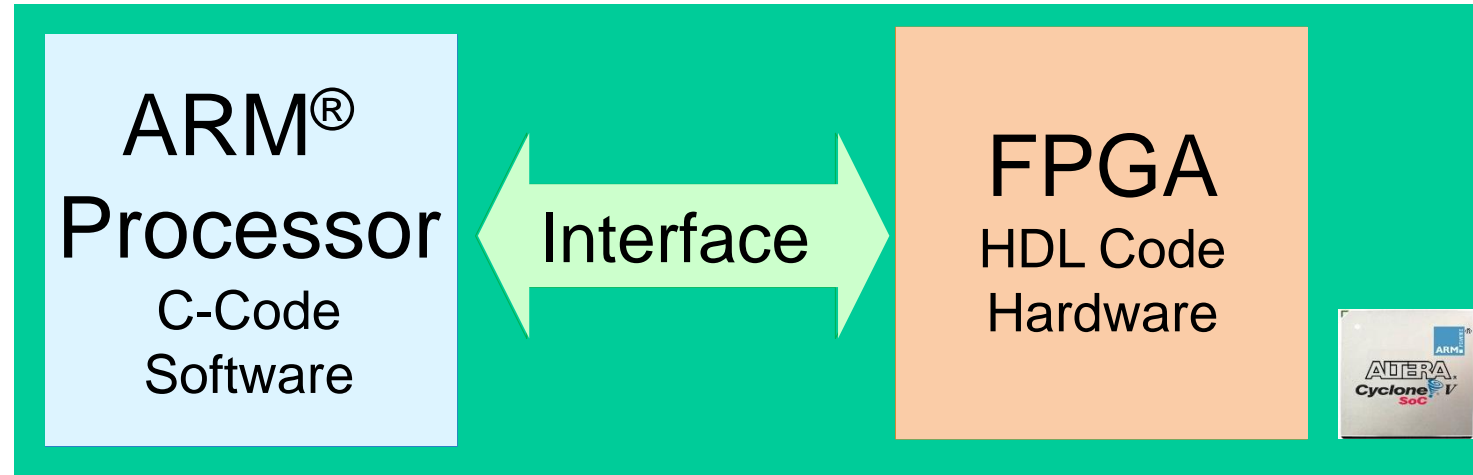


**Deploy design on target system**

# Model-Based Design Workflow for Altera SoCs



# SoC Design Challenge



# SoC Design Challenge

ARM®  
Processor  
C-Code  
Software

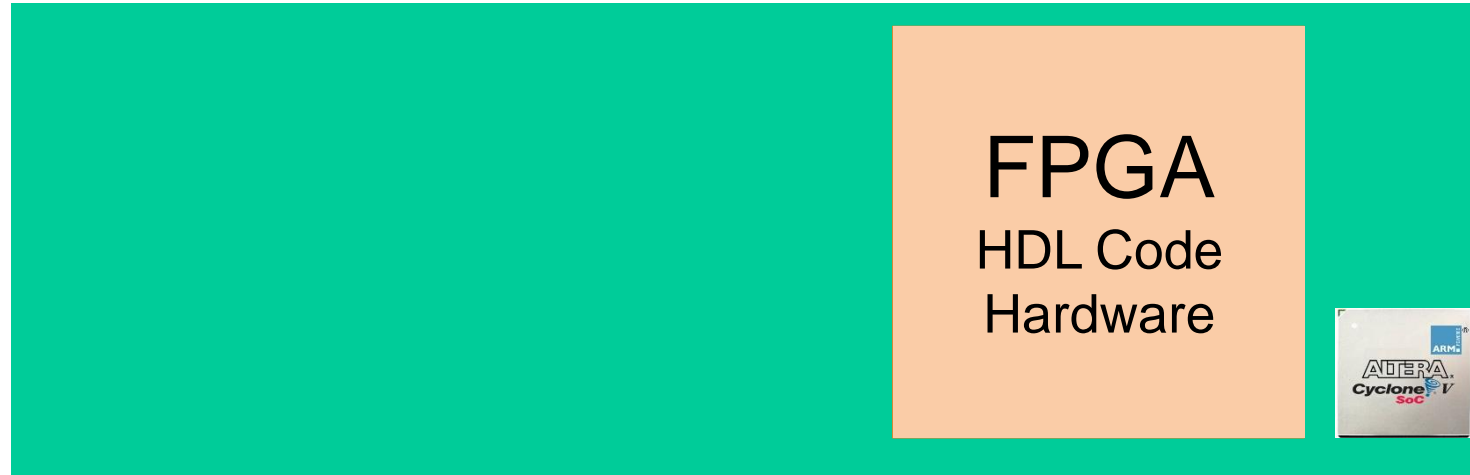


- Typically programmed in C
- Often runs a Linux operating system
- Well-established workflows exist

## CHALLENGES

- FPGA Designers not familiar with programming processors
- What should run on the processor vs. the FPGA?

# SoC Design Challenge

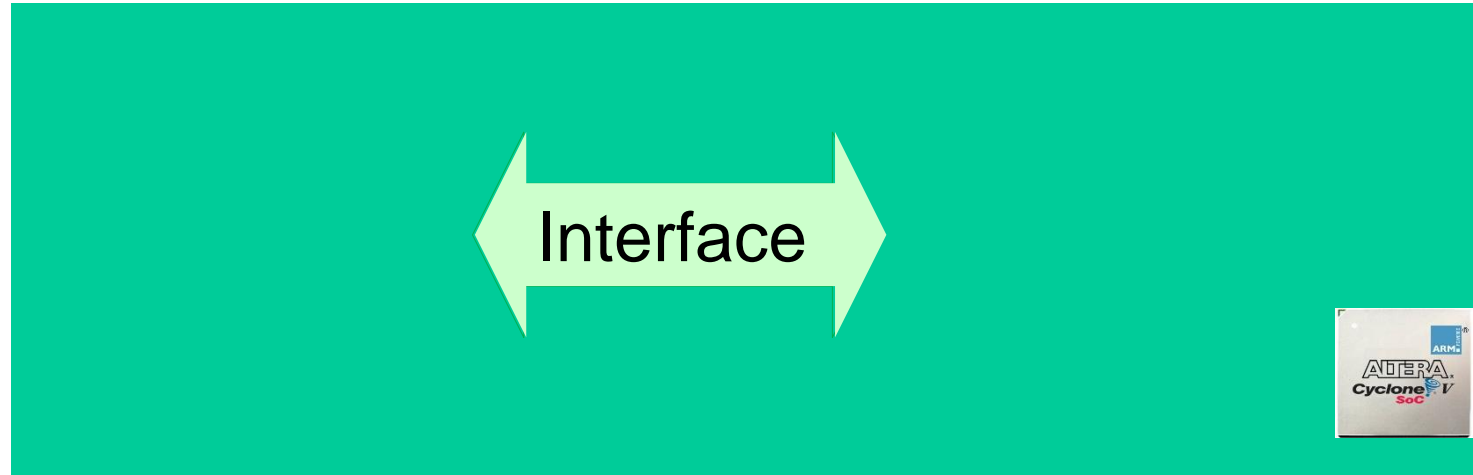


- Typically programmed in VHDL/Verilog
- Established workflows exist

## CHALLENGES

- DSP/Processor programmers not familiar with FPGA Design
- What should run on the FPGA vs. the processor?

# SoC Design Challenge



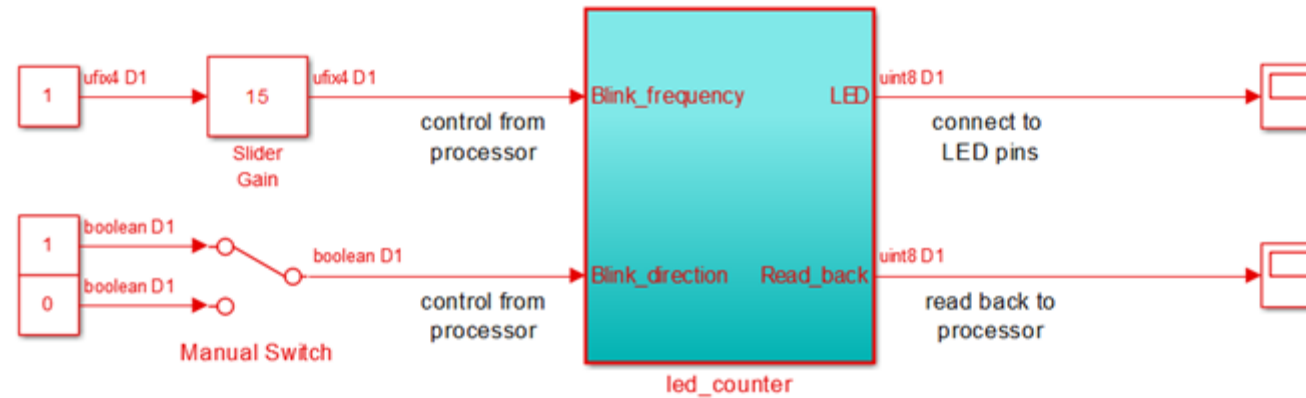
- Altera SoCs use “standard” AXI interface between FPGA and ARM

## CHALLENGES

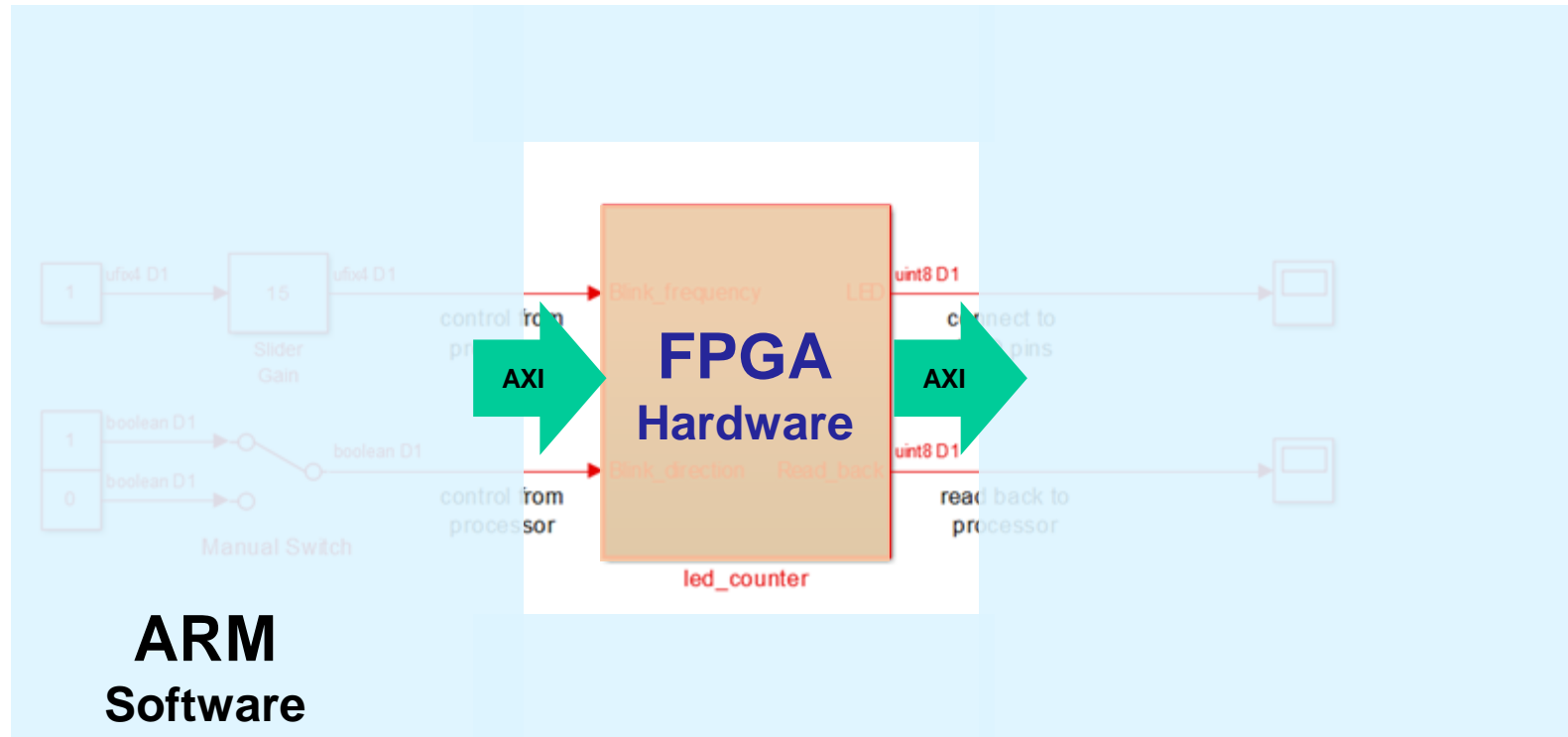
- No established rules for hooking up the interface
- Many different “flavors” of AXI for different bandwidth requirements



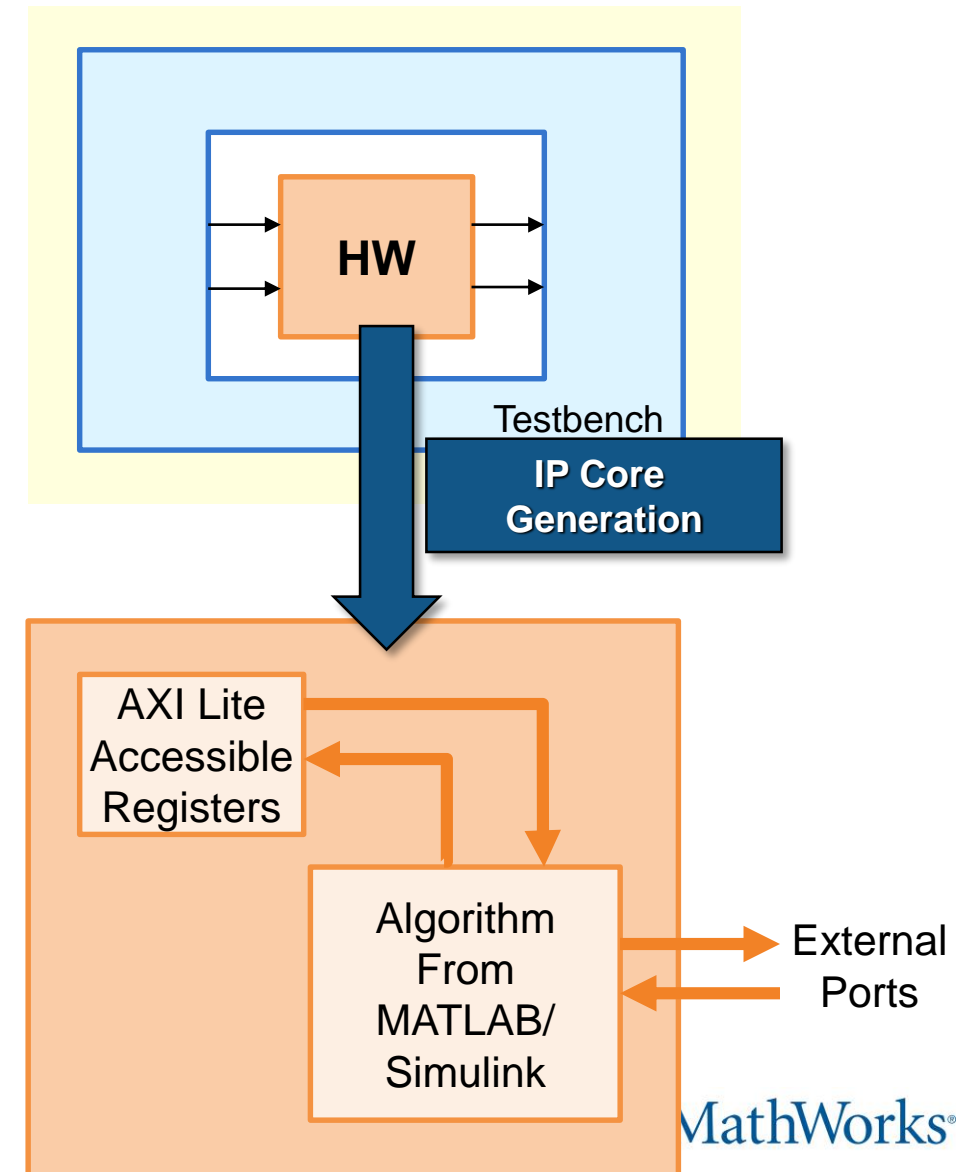
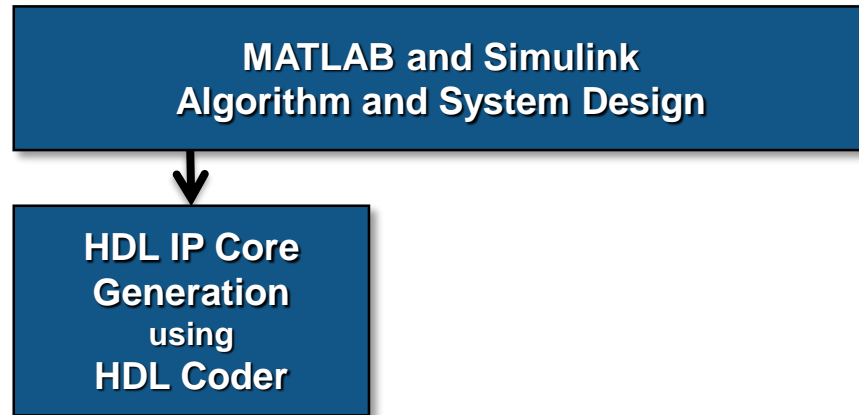
# SoC Model-Based Design Workflow



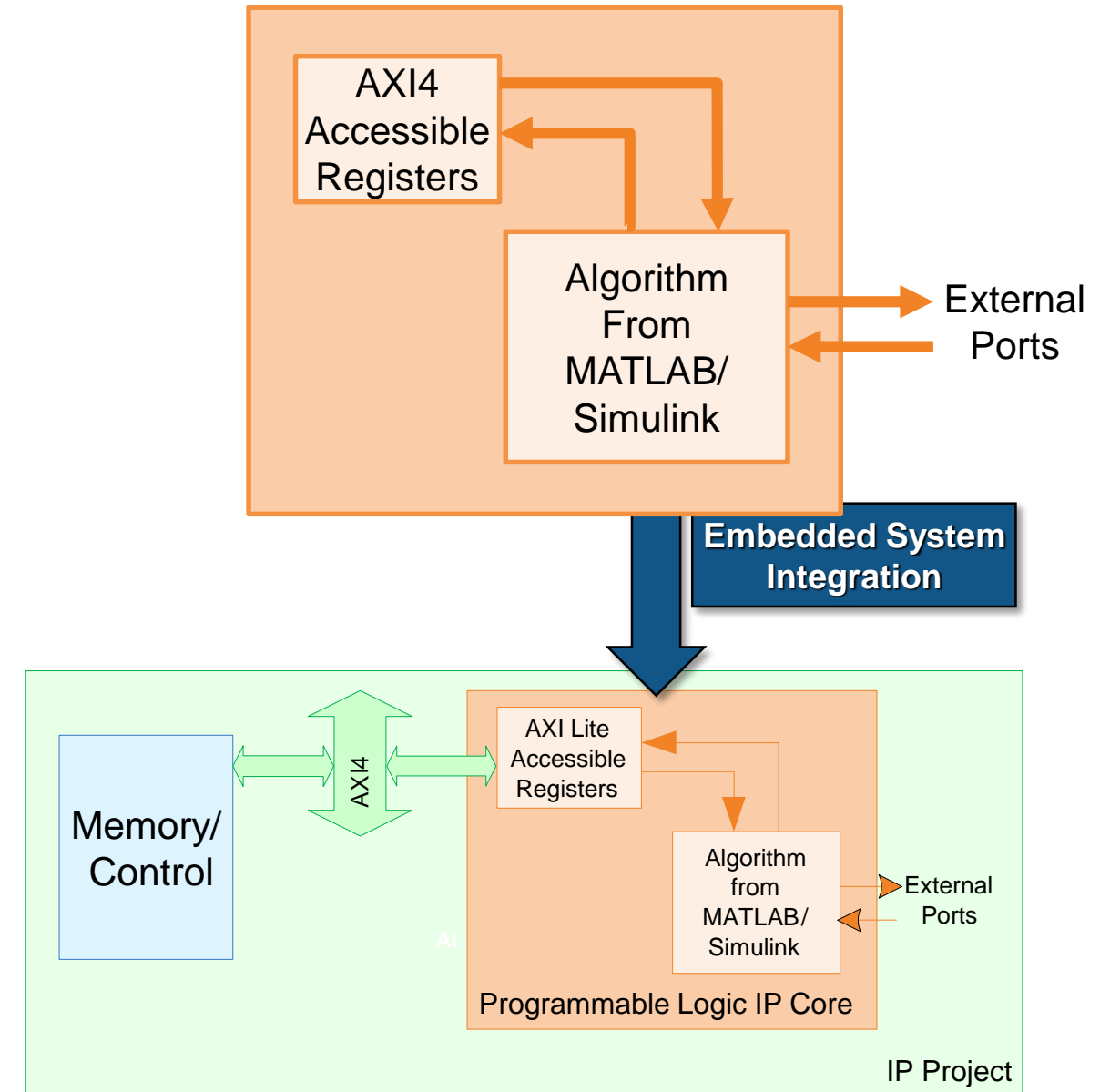
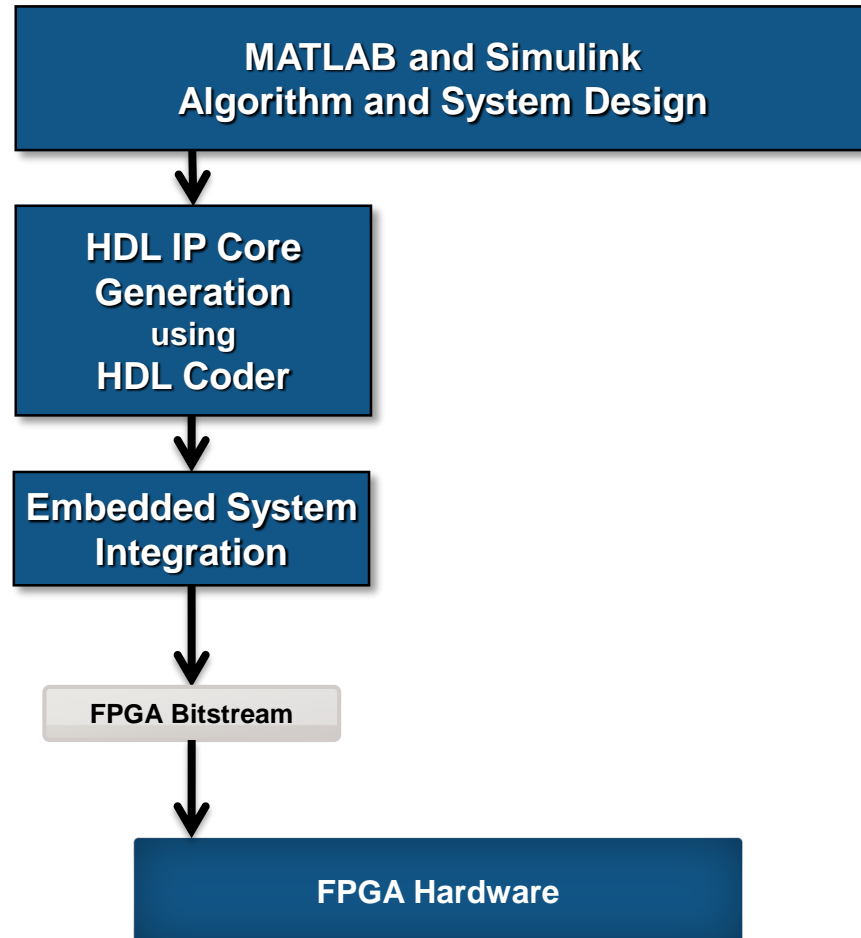
# SoC Model-Based Design Workflow



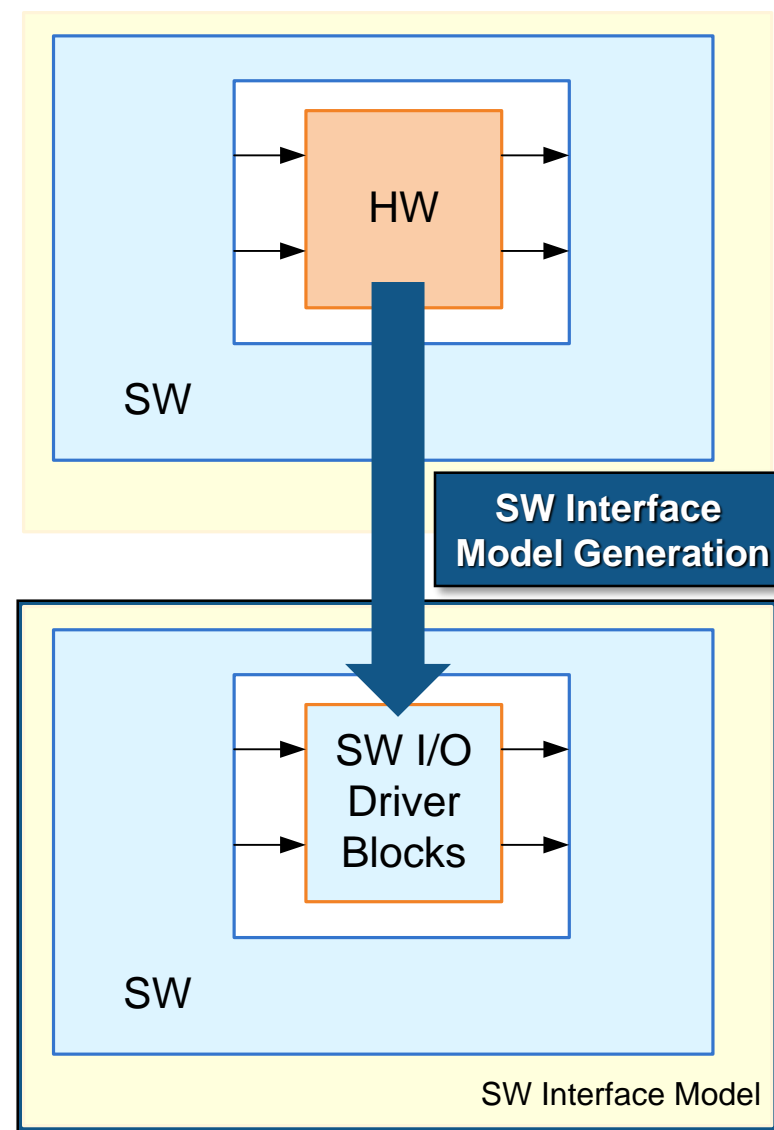
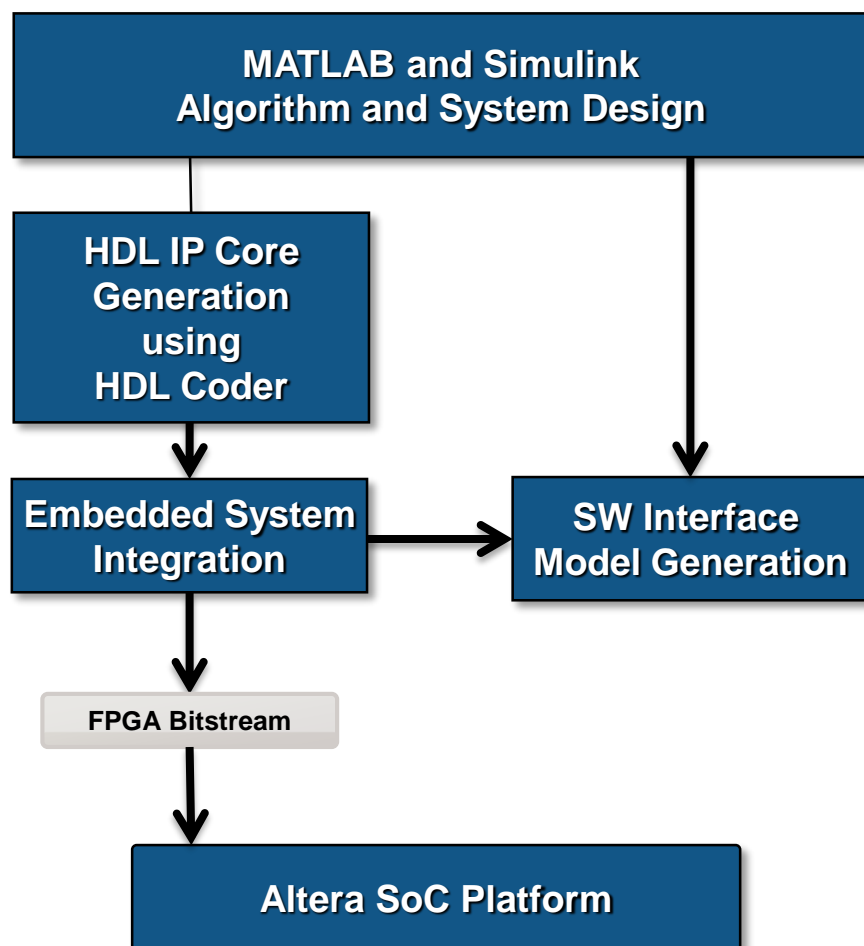
# IP Core Workflow



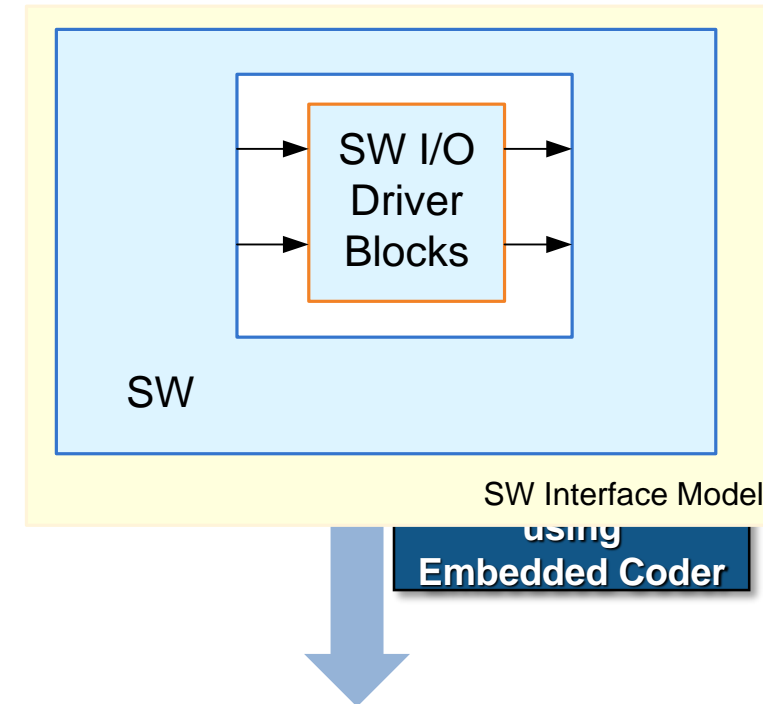
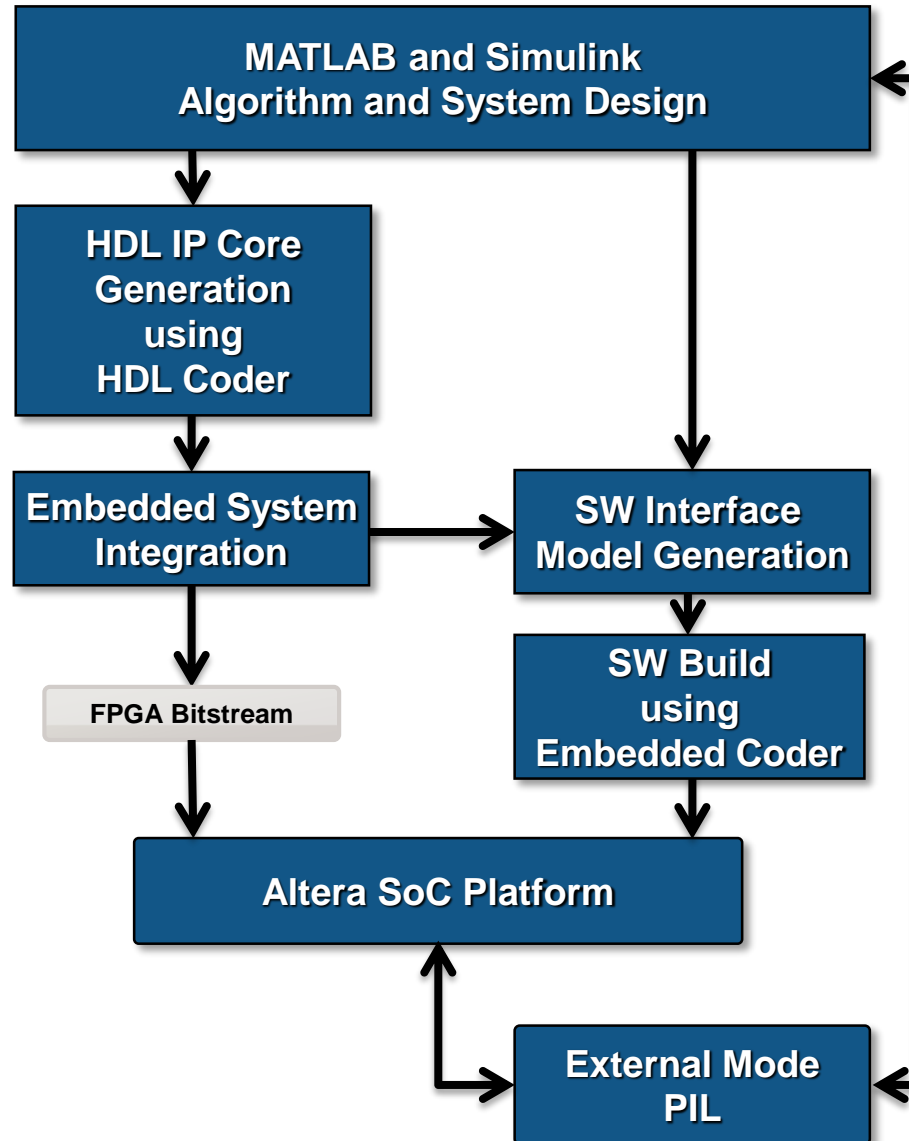
# IP Core Workflow



# SoC Model-Based Design Workflow

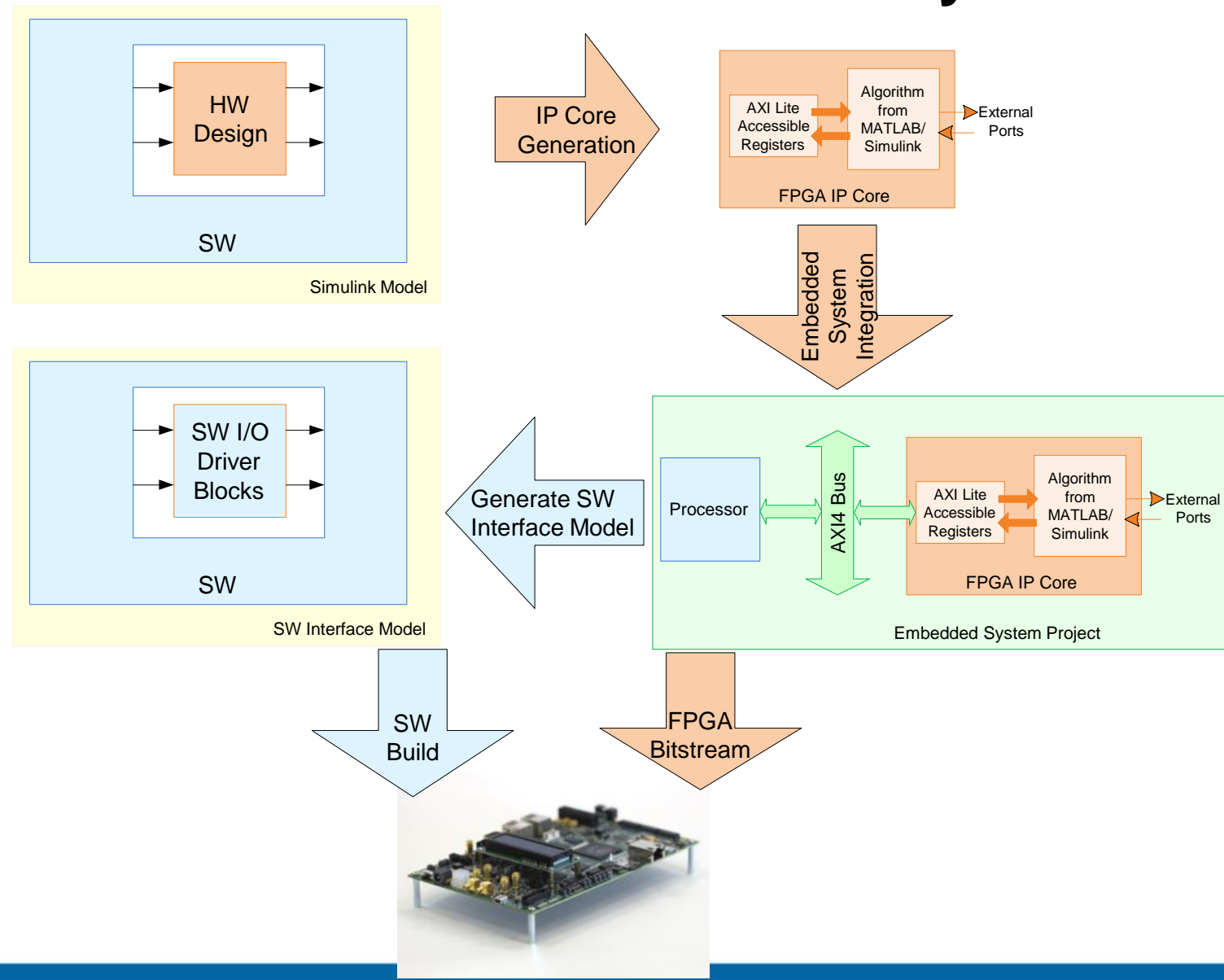


# SoC Model-Based Design Workflow



- Real-time Parameter Tuning and Verification
  - External Mode
  - Processor-in-the-loop

# SoC Hardware/Software Workflow Summary



# Target Platforms Supported with Model-Based Design for Altera SoCs



Altera Cyclone V SoC Development Kit



Arrow SoCKit

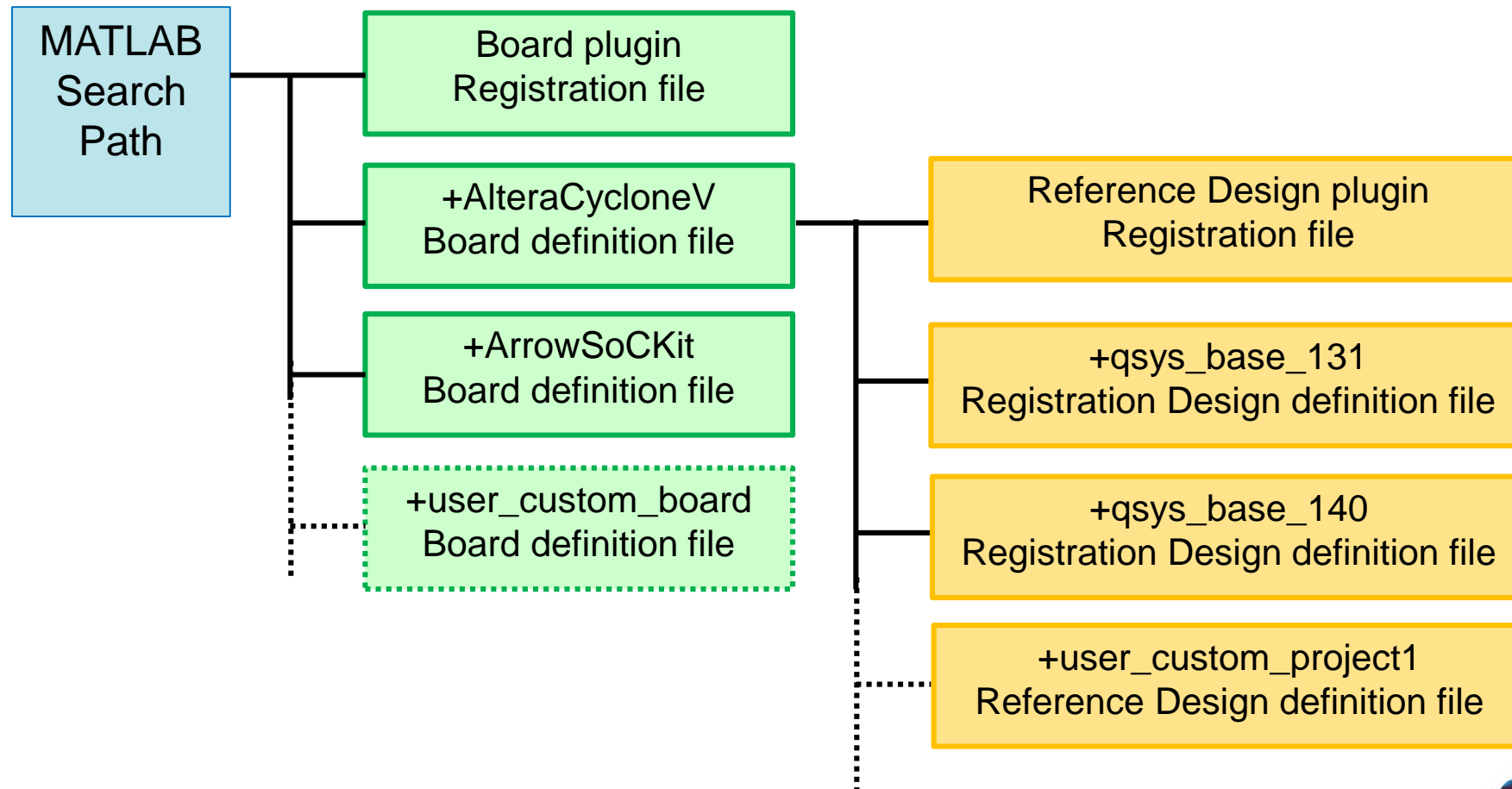


Custom Cyclone V SoC boards

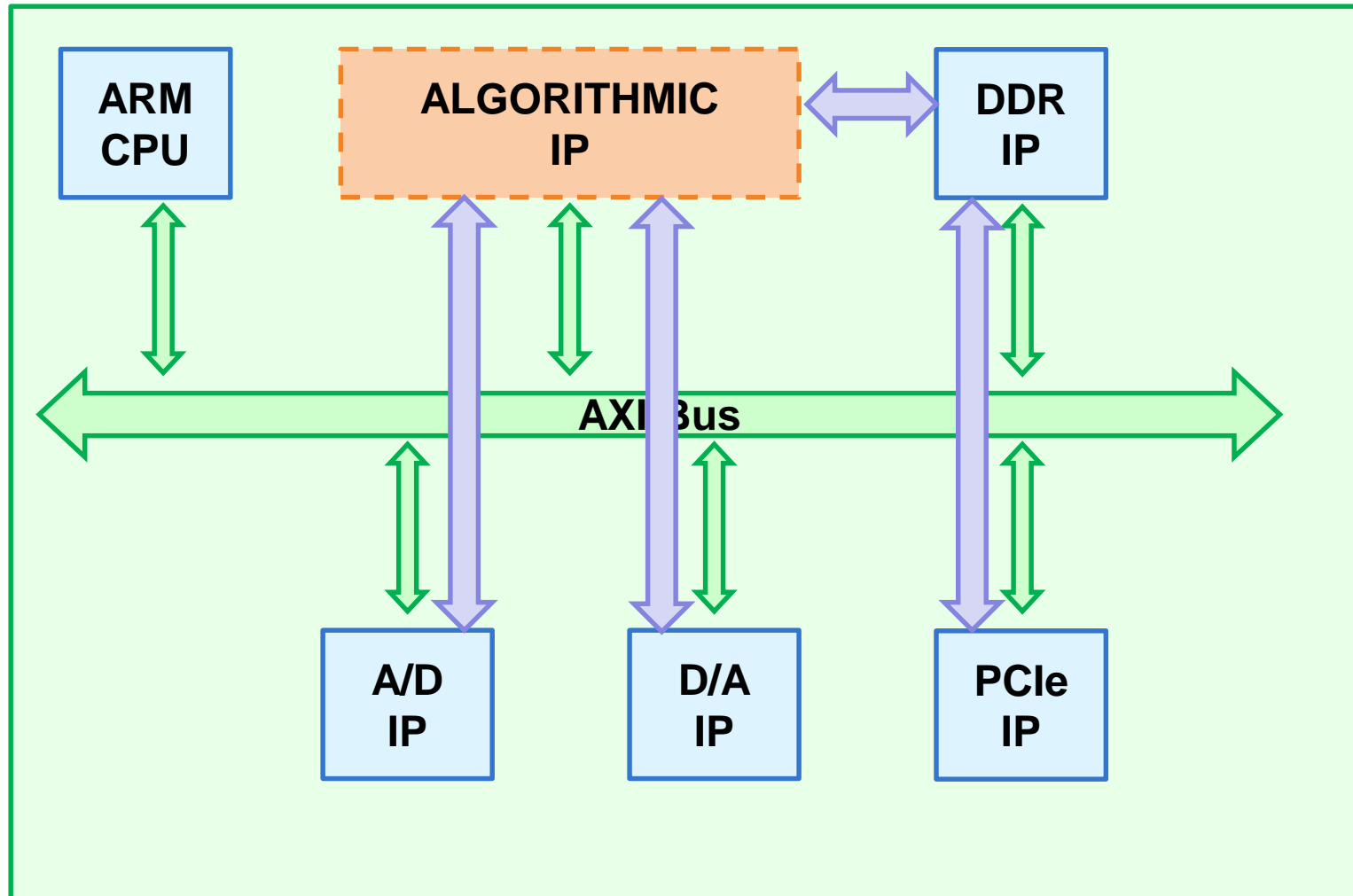


# Adding Support for Custom Altera SoC Boards and Reference Designs

Extensible Board and Reference Design definition



# Reference Design Example



# Summary and Next Steps

- Altera SoC workflow support from MathWorks:
  - Enables combined hardware/software code generation
  - Provides predefined support for on Altera SoC and Arrow SoCKit development boards, and can be extended to other SoC boards.
- Learn more about Model-Based Design for Cyclone V SoCs
  - Visit <http://www.mathworks.com/asdf>
  - Visit [mathworks.com/alterasoc](http://mathworks.com/alterasoc)
  - Contact us at [altera@mathworks.com](mailto:altera@mathworks.com) for instructions on how to get this workflow.
- Watch Altera/MathWorks webinar  
**Prototyping SoC-based Motor Controllers with MATLAB and Simulink**
  - Features targeting field-oriented control algorithm into Altera's Drive-on-a-Chip Reference Design*

The image shows two overlapping screenshots. The top screenshot is from the 'Hardware Support' page on the Altera website, specifically the 'Altera SoC FPGA Support from Embedded Coder' section. It features the Altera logo and a 'Drive-On-Chip Reference Design' banner. The bottom screenshot is a video player interface showing a webinar titled 'Prototyping SoC-based Motor Controllers with MATLAB and Simulink'. The video player includes a 'Table of Contents' sidebar with items like 'Introduction', 'Altera SoCs and Drive-on-a-Chip', 'Model-Based Design for Altera SoCs', 'Demo: Model-Based Design with Drive-on-a-Chip', 'Adding Existing IP and Software', and 'Summary'. The main video area shows a Simulink model and a scope plot. Below the video, the speakers are listed as Eric Cigan (MathWorks) and Ben Jeppesen (Altera). The webinar description states that engineers from MathWorks and Altera will show how to use MATLAB and Simulink to model, simulate, and prototype control systems on Altera Cyclone V SoC devices. It also lists key topics to be demonstrated, such as modeling motor control systems, generating code for Altera Cyclone V SoCs, using MathWorks IP core generation, and downloading programming to an Altera Cyclone V SoC Development Kit.

